CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). An integrated memory, comprising:

a memory cell array of memory cells for storing data;

an access controller for controlling a memory access to said memory cell array for at least one of reading and writing data;

an addressing unit for addressing selected ones of said memory cells corresponding to the memory access based on received addressing signals; and

an addressing calculation logic unit connected to said addressing unit, to be activated by a test mode signal for a test operation of said memory cell array, receiving command signals and address signals for the test operation, calculating the addressing signals from the command signals and the address signals for the memory access, and feeding

the addressing signals into said addressing unit, said addressing calculation logic unit including:

a register unit for storing address parameters for calculating the addressing signals;

a computation cascade connected downstream of said register unit and calculating the addressing signals;

a writing-back logic unit connected downstream of said computation cascade and writing back present addressing signals to said register unit; and

a control unit connected to said register unit and said computation cascade for controlling a calculation process and for feeding initialization values.

Claim 2 (original). The integrated memory according to claim 1, further comprising signal lines receiving signals selected from the group consisting of address signals, command signals, and data signals, during normal operation;

said addressing calculation logic unit receiving the command signals and the address signals for the test operation via said signal lines.

Claim 3 (original). The integrated memory according to claim 1, wherein:

the memory access is synchronized with a clock signal; and

said addressing calculation logic unit calculates the addressing signals in said addressing calculation logic unit within one clock cycle.

Claim 4 (original). The integrated memory according to claim 1, wherein said addressing calculation logic unit has a register for defining at least one of step sizes and jump destinations during the address calculation.

Claim 5 (canceled).

Claim 6 (currently amended). The integrated memory according to claim ~~5~~ 1, wherein said register unit includes an offset register for storing an access start address, a register for storing a present access address, said register unit outputting the present access address to said computation cascade.

Claim 7 (original). The integrated memory according to claim 6, further comprising a redundancy memory cell array;

the access start address stored in said offset register being within said redundancy memory cell array.

Claim 8 (currently amended). The integrated memory according to claim ~~5~~ 1, wherein said computation cascade receives an address of said register unit, has a register for storing a parameter value, has an addition unit for adding the parameter value to the received address to form a modified address and outputs the modified address, has a bypass with respect to said addition unit for outputting the received address unchanged.

Claim 9 (original). The integrated memory according to claim 8, wherein said addition unit is at least one of an adder for adding and a subtracter for subtracting.

Claim 10 (original). The integrated memory according to claim 8, wherein said control unit controls when the received address is modified.

Claim 11 (original). The integrated memory according to claim 8, wherein said control unit controls when addition of at least one of the parameter values is effected.

Claim 12 (original). The integrated memory according to claim 8, wherein said control unit controls when subtraction of at least one of the parameter values is effected.

Claim 13 (original). The integrated memory according to claim 8, further comprising a comparison logic unit connected downstream of said computation cascade for comparing a predetermined maximum value of an address with an output address of said computation cascade; the output address being fed in modified form into said addressing unit for the memory access depending on a comparison result.

Claim 14 (canceled).

Claim 15 (currently amended). ~~The integrated memory according to claim 14, wherein~~ An integrated memory, comprising:

a memory cell array of memory cells for storing data, said memory cell array having rows and columns with said memory cells disposed at crossover points of said rows and columns;

an access controller for controlling a memory access to said memory cell array for at least one of reading and writing data;

an addressing unit for addressing selected ones of said memory cells corresponding to the memory access based on received addressing signals; and

an addressing calculation logic unit connected to said addressing unit, to be activated by a test mode signal for a test operation of said memory cell array, receiving command signals and address signals for the test operation, calculating the addressing signals from the command signals and the address signals for the memory access, and feeding the addressing signals into said addressing unit; said addressing calculation logic unit ~~includes~~ including:

a register unit with separate registers in each case for storing row and column address parameters for calculating ~~the~~ row ~~address~~ addresses and ~~the~~ column ~~address~~ addresses;

a multiplexer connected to said register unit;

a computation cascade connected downstream of said register unit via said multiplexer and serially calculating the row and column addressing signals;

a writing-back logic unit connected downstream of said computation cascade and serving for respectively writing back present row and column addressing signals to said register unit; and

a control unit connected to said register unit ~~(21)~~ and said computation cascade for controlling a calculation process and for feeding in initialization values.

Claim 16 (original). A method for checking an integrated memory, which comprises:

providing an integrated memory according to claim 1;

activating the addressing calculation logic unit for a test operation by a test mode signal;

initializing the integrated memory with a transfer of initial parameters to be stored into the addressing calculation logic unit; and

after the initializing step, applying the command signals and the address signals for the test operation to the addressing calculation logic unit and carrying out read/write operations with the access controller.

Claim 17 (original). The method according to claim 16, which further comprises, with the initializing, transferring an address within a redundancy memory cell array as an access start address to the addressing calculation logic unit.